REMARKS

Summary of Office Action

Claims 1-19, 21-30, and 32-39 were pending in the above-identified patent application.

Claims 1-13, 18-19, 21-30, and 32-39 were rejected under 35 U.S.C. § 102(b) as being anticipated by Co et al. U.S. Patent No. 5,631,587 ("Co"). Claims 14-17 were rejected under 35 U.S.C. § 103(a) as being obvious from Co in view of Brunn et. al. U.S. Patent No. 6,650,195 ("Brunn").

Summary of Applicants' Reply

Applicants have amended claims 1, 2, 18, 19, 29, and 30 to more particularly define the invention, canceled claim 3 without prejudice, and added new claims 40-46. No new matter has been added and the amendments are fully supported by the originally filed specification (see, e.g., applicants' specification at FIG. 2A; pp. 13-14, ¶¶ 32 and 33; and p. 11, ¶ 27).

The Examiner's rejections are respectfully traversed.

Applicants' Reply to the Rejection of the Claims

Claims 1, 2, 4-13, 15, 18, 19, 21-30, and 32-39 were rejected under 35 U.S.C. § 102(b) as being anticipated by Co. Claims 14-17 were rejected under 35 U.S.C. § 103(a) as being obvious from Co in view of Brunn.

Claims 1, 2, and 4-17

Applicants' amended independent claim 1 is directed to circuitry operative in two modes for providing a

dynamically adjustable bandwidth. The circuitry includes, among other things, a phase frequency detector that receives as input a clock signal and a phase detector that receives as input a clock data recovery (CDR) signal. A charge pump has a pump input coupled to the signal output of the phase frequency detector during a first of the two modes, and has the pump input coupled to the signal output of the phase detector during a second of the two modes.

Co describes a method for providing an output signal at an output frequency in response to an input signal at an input frequency. (See, e.g., Co, col. 1, ll. 55-65, col. 3, ll. 54-64, and col. 5, ll. 9-25.)

The Examiner cited to FIGS. 3 and 6 of Co as allegedly showing all the limitations of applicants' claim 1. Office Action, pp. 2-3.

Applicants respectfully submit that Co does not show or suggest a phase detector that receives as input a CDR signal, and a charge pump with a pump input coupled to the signal output of the phase frequency detector during a first of two modes, and coupled to the signal output of the phase detector during a second of two modes, as defined by applicants' claim 1. Instead, as shown and described in FIG. 6 of Co, phase/frequency detector 300 is coupled to the input signal and provides a difference signal between the input and output signals to a charge pump 400. Clearly, the charge pump is only coupled to the output of the phase detector. Nowhere does Co show or suggest a phase frequency detector and a phase detector that are coupled to the charge pump in a first and a second mode, respectively.

Further, in Co, phase detector 300 receives from frequency divider 100 an input frequency signal, which is clearly not a CDR signal. Nowhere does Co show or suggest a phase detector that receives as input a CDR signal and has a signal output. Brunn, which is cited by the Examiner as allegedly showing limitations of applicants' dependent claims, does not make up for the deficiencies of Co in that regard.

Therefore, at least because Co does not show or suggest a circuit operative in two modes, where a charge pump has its input coupled to the signal output of the phase frequency detector during a first mode, and has its input coupled to the signal output of the phase detector (which receives an input CDR signal) during a second of the two modes, and because Brunn does not make up for the deficiencies of Co, neither Co nor Brunn, whether taken alone or in combination shows or suggests all the features of applicants' claim 1. Therefore, applicants respectfully submit that claim 1 and its dependent claims 2 and 4-17 are patentable.

Claims 18, 19, 21-30, and 32-39

Applicants' amended independent claims 18 and 29 are directed to a programmable logic device having a clock data recovery (CDR) circuitry (claim 18) or phase locked loop (PLL) circuitry (claim 29), each being selectively operative in two modes, and control circuitry. The CDR/PLL circuitry uses a clock signal to produce a recovered clock signal having a phase and frequency which correspond to the phase and frequency of the clock signal when a first of the two modes is selected. When a second of the two modes is selected, the recovered clock signal is used to recover clock information

and data information from a CDR signal (claim 18) or is used to drive another component external to the CDR/PLL circuitry in the programmable logic device (claim 29).

The Examiner cited FIGS. 3 and 6 of Co as allegedly showing all the limitations of applicants' claims 18 and 29. Office Action, pp. 4 and 7.

Applicants respectfully submit that Co does not show or suggest, among other things, a programmable logic device that is selectively operative in two modes and has CDR/PLL circuitry, where in a first selected mode the CDR/PLL circuitry uses a clock signal to produce a recovered clock signal and in a second selected mode the recovered clock signal is used to recover information from a CDR signal or drive another component external to the CDR/PLL circuitry in the programmable logic device, as defined by applicants' claims 18 and 29. Instead, in Co the phase-locked loop and phase-locked loop adjustment circuit merely operate to "generate an output signal at an output frequency in response to an input signal at an input frequency" (Co, col. 1, l. 67 to col. 2, l. 2). Nowhere does Co show or suggest that the phase-locked loop is selectively operative in two modes, where in the first mode the phase-locked loop uses a clock signal to produce a recovered clock signal and in a second mode the recovered clock signal is used to recover information from a CDR signal or drive another component external to the phase-locked loop in the programmable logic device. At most, the phase-locked loop in Co merely has one mode of operation. Furthermore, Co does not even show or suggest that the phase-locked loop is in a programmable logic device. Clearly,

Co does not show or suggest, and therefore cannot anticipate, all the features of applicants' claims 19 and 29.

Therefore, applicants respectfully submit that independent claims 18 and 29 and claims 19, 21-28, 30, and 32-39 which depend, directly or indirectly, therefrom are patentable.

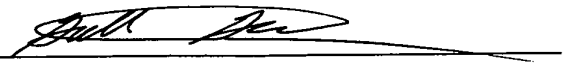
New Claims

Applicants have added new claims 40-46 to more particularly define the invention. Claims 40-46 depend, directly or indirectly, from patentable claims 1, 18, or 29 and therefore are also patentable.

Conclusion

Applicants respectfully submit that this application is in condition for allowance. Accordingly, reconsideration and prompt allowance of this application are respectfully requested.

Respectfully submitted,



Gall C. Gotfried
Registration No. 58,333
Agent for Applicants
FISH & NEAVE IP GROUP
ROPES & GRAY LLP
Customer No. 36981
1251 Avenue of the Americas
New York, New York 10020-1105
(212) 596-9000